REMARKS

In a final office action dated 4 June 2004, the Examiner also rejects claims 1-7 (all pending claims) and objects to the drawings. In response to the office action, Applicants amend claims 1, 4 and 7. Applicants also cancel claims 2 and 5. Furthermore, Applicants also respectfully traverse the rejections of claims 1-7 (all pending claims). Claims 1, 3, 4, 6, and 7) remain in the application. In light of the arguments set forth below, Applicants respectfully request that all objections and rejections be removed and the application be allowed.

A redlined correction is submitted showing the proposed amendment to Figure 3 to correct the informality. Formal drawings including all corrections will be furnished with allowance of the Application.

The Examiner rejects claim 1 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 6,442,446 issued to Nakamura et al. (Nakamura) in view of U.S. Patent Number 5,179,670 issued to Farmwald et al. (Farmwald) in further view of what is well known in the art as exemplified by any one of U.S. Patent Application Publication Number 6,283,227 applied for by Appleby-Allis et al. (Appelby), U.S. Patent Number 6,283,227 B1 issued to Lerche et al. (Lerche), U.S. Patent Number 6,009,409 issued to Adler et al. (Adler), and U.S. Patent Number 5,986,465 issued to Mendel (Mendel). In order to maintain a rejection the Examiner has the burden of providing evidence of prima facie obviousness. See MPEP §2143. See also In Re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). In order to prove prima facie obviousness, the Examiner must provide evidence in the prior art of a motivation to combine or modify a reference, a reasonable expectation of success, and a teaching of each and every claimed element. Id.

Amended claim 1 recites a master programmable device that has a revision register with memory locations with each memory location storing revision information for a particular programmable slave device. Nakamura does not teach this limitation. Instead, Nakamura teaches machine controllers which execute programs for controlling a semiconductor wafer processing apparatus. (See Col. 3, line 62-Col. 4, line 14). Nakumura does teach storing the revision information for applications executed by slave devices. However, the section cited in Nakumura that teaches storing revision information does not teach storing the information for each slave device in a memory space that is specifically reserved for storing revision information for a particular slave device. Nakumura is teaching software performing the process that stores the revision information in memory accessible by the application. However, in the invention in claim 1, the use of particular addresses for storing the revision information for a particular device is important so that the information may be accessed by other equipment used for teaching and debugging that may be reading the information when the master device is not operating. Thus, the revision register claimed in claim 1 is not taught in Nakumura. Thus, Nakamura does not teach the limitations of the master device and the at least one slave device as recited in amended claim 1.

Farmwald also does not teach the master and slave devices that are either a field programmable gate array or an erasable programmable logic device as recited in claim 1. Farmwald does not mention that a master device receives revision information and stores the information from each slave device in particular memory location that stores the revision information for a particular slave device. Farmwald merely teaches the use of pulses transmitted along a bus and mentions no applications for data being transmitted along the bus. Thus, Farmwald does not teach the master and slave devices recited in amended claim 1.

None of the art cited as showing that an FPGA or other programmable device teaches the use of particular memory locations in a register. Appelby teaches a system for controlling peripheral hardware and programming FPGA in the Hardware. There is no mention in Appelby of using particular memory location to store information for a particular slave device. Lereche teaches a system for assigning identifiers in a downhole activation system that is provided by a software system. There is no mention in Lereche of using particular memory locations to store information about a particular device. Adler teaches a system and method for displaying advertising in a communications network. Adler teaches a software application that schedules and displays the advertising on processing systems in a network. There is no mention anywhere in Adler of having a memory that has particular memory location for storing particular information for a device. Mendel teaches a programmable logic that incorporates a global sharable expander. However, Mendel does not teach having a memory that has specific locations for providing specific information about a device. Thus, none of the references teach the revision register claimed in amended claim 1.

Since none of the cited references teaches a master programmable device having a revision register having memory locations that each store revision information for a particular slave device as recited in amended claim 1, the combination of Nakamura, Farmwald and any of the references including Appelby, Lereche, Adler, and Mendel does not teach the master and slave devices recited in amended claim 1. Therefore, Applicants respectfully request that the rejection of claim 1 be removed and amended claim 1 be allowed.

Even if the references could be combined to perform in the manner stated by the Examiner, The Examiner has provided no motivation to do so as required by case law

and the MPEP. See MPEP §2143. The Examiner is reminded that for a combination to be proper the proposed modification or combination cannot change the principle mode of operation of reference. See MPEP §2143.01 See also In re Ratti, 270 F2d. 810 (CCPA 1959).

The combination proposed by the Examiner would change the principle of operation of Nakumura. Nakamura teaches machine controllers which execute programs for controlling a semiconductor wafer processing apparatus. (See Col. 3, line 62-Col. 4, line 14) Although it is not explicitly stated, these controllers must be processing units in order to execute programs since the controllers execute programs. The process in Nakumura works properly where the master and slave controllers have the processing capacity and memory to perform the applications needed to perform the method taught. However, these functions may not work where processing capacity and memory are at premium. As can be seen by the references cited by the Examiner there are some cases where applications performed by a processor may be replaced by programmable circuitry. However, there is no suggestion in Nakumura itself that the controllers may by replaced by programmable logic. Furthermore, Nakumura is teaching a system in which revisions to revisions of applications are being maintained and not the configuration of programmable devices which are different. Thus, the modification of Nakumura proposed by the Examiner is improper and the rejection should be removed. Thus, Applicants respectfully request amended claim 1 be allowed.

Claim 3 is dependent upon amended claim 1. Therefore, claim 3 is allowable as being dependent upon an allowable independent claim. Thus, Applicants respectfully request that the rejection of claim 3 be removed and claim 3 be allowed.

The Examiner rejects claim 4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 6,442,446 issued to Nakamura et al. (Nakamura) in view of the admitted prior art. In order to maintain a rejection the Examiner has the burden of providing evidence of prima facie obviousness. See MPEP §2143. See also In Re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). In order to prove prima facie obviousness, the Examiner must provide evidence in the prior art of a motivation to combine or modify a reference, a reasonable expectation of success, and a teaching of each and every claimed element. Id.

Claim 4 recites the same revision register and memory location recited in amended claim 1. Thus, Nakumura does not teach the storing of revision information in the memory locations as recited in amended claim 4. Furthermore, the admitted prior art does not teach this limitation. Since neither Nakumura nor the admitted prior art teach this limitation, the combination of Nakumura and the admitted prior art does not teach this limitation. Thus, the rejection should be removed and amended claim 4 be allowed.

Furthermore, even if the combination does teach amended claim 4. The combination is improper for the same reasons as expressed with regards to amended claim 1. Thus, the rejection should be removed and amended claim 4 be allowed.

Claim 6 is dependent upon amended claim 4. Therefore, claim 6 is allowable as being dependent upon an allowable independent claim. Thus, Applicants respectfully request that the rejection of claim 4 be removed and claim 6 be allowed.

Amended claim 7 has been amended to claim the process performed by the system recited in amended claim 1. Thus, the rejection to claim 7 is moot and amended claim 7 is

allowable for at least the same reasons as amended claim 1. Therefore. Applicants respectfully request that amended claim 7 be allowed.

If the Examiner has any questions about this response or the claims in general, the Examiner is invited to telephone the undersigned at 775-586-9500.

Respectfully submitted,
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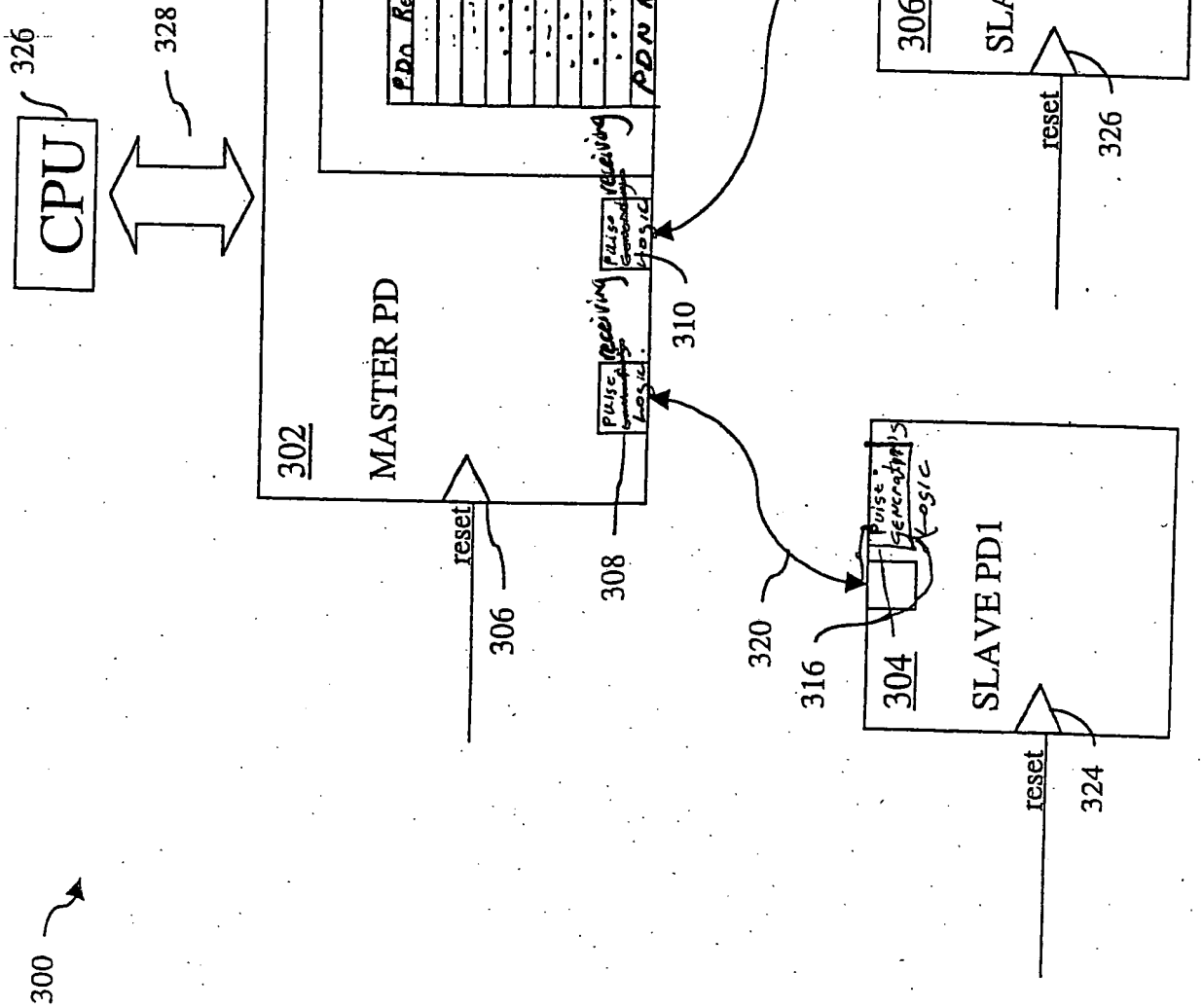

FIG. 3A